ANALYSIS AND ENHANCEMENT OF TRANSIENT STABILITY IN DIFFERENT HVDC CONFIGURATIONS

تحليل و تدعيم الإستقرار العابر بأشكال نظم الجهد الفائق المستمرالمختلفة

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لملخص: نمت محاكاةالعديد من سيناريوهات نشوء الحالات العابرة لنظام الجهد الفائق المستمر و تحليل إداء النظام و دراسة إستقراره العابر. وكـد تـم الأخذ فى الاعتبار تأثير التوصيل و الفصل المفاجيء للأحمال عند طرق التحكم المختلفة. كما تم دراسة الأداء العابر عند فصل خط التيار المتردد الموصل بالتوازى مع خط الجهد المستمر فى الأنظمة من النوع (SIFAC) وكذا نصل خط التيار المتردد الذى يربط العاكسين من الجهد المستمر إلى المتردد فـى الأنظمة من النوع (MIF). و تم دراسة الأداء العابر عند حدوث إنخفاض مفاجيء للجهد المتردد نتيجة قصر بخط التيار المتردد. و نمت دراسة محسنات الأداء العابر باستخدام وسائل نحسين التحكم فى انظمة الجهد المستمر وكذا عن طريق إبخال لقدرة غير فعالة عند العاكس.

Abstract: - The performance of the High Voltage Direct Current transmission system "HVDC" is defined from a transient stability perspective making it possible to issue adequate corrective actions with suitable extent according to the actual transient condition. Transient originating scenarios in HVDC systems were simulated and the system's stability performance was accordingly analyzed. Analysis included the effect of sudden application and removal of different load types at different control modes, breaking the parallel AC line in single infeed AC systems or the line connecting two inverters in multi infeed systems, and short-circuit originated voltage dips.

1 Introduction

HVDC system transient stability is the ability of the HVDC system, for a given initial operating condition, to regain state of operating equilibrium after being subjected to a transient disturbance, with system variables bounded to normal operating limits. Transient stability of the system is thus affected by the system's initial operating state, the kind and severity of disturbance, and the response of some of the HVDC system controls. The transient disturbance is expected to affect DC and AC system parameters as well [1], the former having a direct bearing on the counter control action or control mode choice, while the later affects the stability of the AC adjacent system. The most significant parameters for the AC system will be the AC voltage and its phase shift, whereas the DC current and voltage provide the main inputs to HVDC rectifier and inverter controls.

Several researches investigated HVDC transient stability, either from HVDC system parameters response perspective or as a part of the entire AC-DC power system. Furthermore, the effect of alternative DC link position with respect to the AC network was analyzed [2, 3]. Framework models for transient and steady state stability as well were proposed. Taking into consideration the importance of the initial and final operating states to transient stability analysis, static and small signal stabilities were addressed; the former for being associated with the pre-disturbance initial operating state, as well as the settling state in case of a transiently stable condition, while the later for being associated with control order level changes liable to take place in response to the disturbance. Both of the voltage dependent current order limit, "VDCOL" and static VAR compensator, "SVC", are used to improve transient stability at sudden load

changes. VDCOL is applied to lower the controller current order during prolonged low AC voltage conditions thus reducing the probability of commutation failure and causing recovery of AC voltage through reduction of converter's reactive power demand [4].
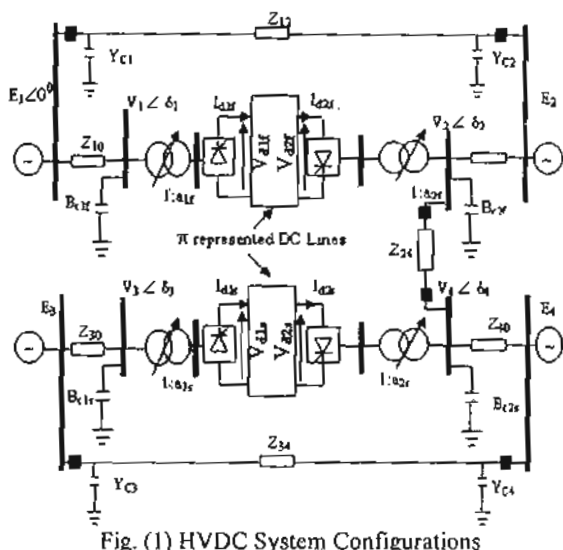
In this paper, the sudden changes of dynamic and static loads [5] connected to converter bus are modeled and their effects are further analyzed for single infeed, "SIF" and single infeed parallel with AC line, "SIFAC" configurations [6]. Furthermore, transients due to the reduction of parallel connected AC lines in SIFAC and AC lines connecting inverters in multi infeed HVDC systems, "MIF" [7] are presented and analyzed. Different related corrective control actions and / or compensation are modeled and their effects on the response of system parameters are analyzed accordingly.

2 HVDC System Configurations

Different configurations are obtained by modifying the AC connections of the general test system shown in fig. (1) according to table 1; where (E_1, E_2, E_3, E_4) and (V_1, V_2, V_3, V_4) are AC line voltages (and terminals as well) at infinite buses and converters respectively.

Table 1: Realization of HVDC Configurations

HVDC Configuration	Disconnected AC Lines
SIF	(E_1, E_2) , (E_3, E_4) & (V_2, V_4)
SIFAC	(V_2, V_4)
MIF	(E_1, E_2) & (E_3, E_4)

Fig. (1) HVDC System Configurations

3 Solution Methodology

The system's differential algebraic equations are solved according to the following algorithm:

1.   The system's differential equations are solved using 4th order "Runge-Kutta" method with a time step of 10 μsec.
2.   The DC system variables obtained from differential equations' solution are used to calculate the active and reactive powers at converter buses.
3.   The calculated active/reactive powers are included in the AC-DC system equations.
4.   The system's AC-DC power flow equations are solved using Newton-Raphson method.
5.   The AC line voltages and their angles are updated to their new values.
6.   Steps from (1) to (5) are repeated until final time of simulations is reached.

4   Transient Disturbances

To analyze transient disturbances, the system data and per unit bases used by Padiyar and Rao are adopted [8].

4.1 Sudden Load Changes

When the static load connected at the converter bus encounters a sudden change, the converter buses' voltage and consequently the entire HVDC system performance will be affected due to this transient condition.

Fig. (2) illustrates the transient behavior of AC and DC system parameters due to a sudden doubling of the inverter's side static load coefficients at 0.1 sec. The considered HVDC system is SIF at $ESCR_{Inv}$ of 2.015 and VSF_{Inv} of 0.465, close to HP (weak AC system), adopting CC/Cβ control mode. The DC line current at the rectifier's side was found to have a small oscillation

compared with the inverter's side DC line current. This outcome is due to the effect of CC control at rectifier. The figure illustrates also the transient responses of DC and AC line voltages, the rectifier firing angle and the response of static active and reactive load at inverter bus.

Fig. (2) Transient behavior of AC and DC system parameters due to a sudden doubling of the inverter's side static load coefficients at 0.1 sec. (SIF at $ESCR_{Inv}$ of 2.015 on CC/Cβ.)
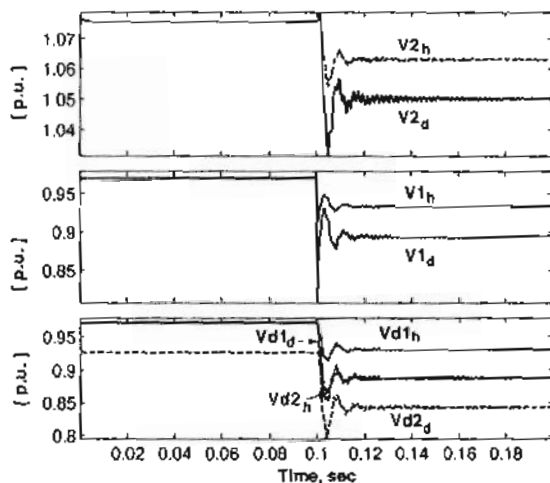

Fig. (3) Transient behavior of AC and DC system parameters due to sudden 50% and 100% increase of the rectifier's side static load coefficients at 0.1 sec. (SIF at $ESCR_{Rect}$ of 2.993 on CDA/CC.)
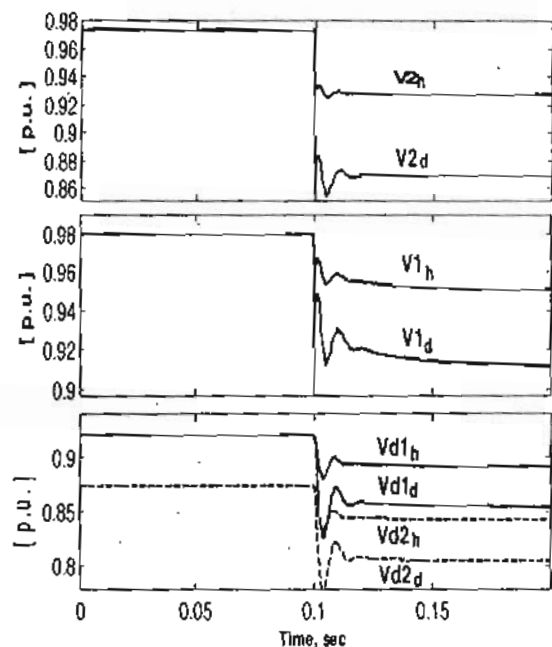
Fig. (4) Transient behavior of AC and DC system parameters due to sudden 50% and 100% increase of the inverter's side static load coefficients at 0.1 sec. (SIFAC at $ESCR_{Inv}$ of 2.39 on CP/Cβ.)

Figures (3) and (4) illustrate the AC and DC system parameters' transient behavior due to 50% and 100% sudden increase of rectifier and inverter sides static load coefficients at 0.1 sec respectively. The SIF system adopts CDA/CC control mode at $ESCR_{Rect}$ 2.993, while SIFAC adopts CP/Cβ control mode at $ESCR_{Inv}$ 2.39.

In Fig. (3), the AC line voltages decreased with AC load sudden increase in such a way that lead to a drop in DC line voltages. The current controller at the inverter side increased the inverter's advance angle and decreased its firing angle to overcome the reduction of DC line voltage. A similar behavior is illustrated by Fig. (4); the power controller at rectifier decreased the rectifier's firing angle to maintain the DC line voltage at a higher level.

Fig. (5) illustrates the corrective effect of installing an SVC at rectifier AC bus or applying VDCOL compared with the system's response without any addition. When the SVC is installed, reactive power is inserted to the AC system, the rectifier's AC line voltage is improved and consequently the DC line voltage. The VDCOL decreases the current controller order and consequently decreases the DC line current causing a consequent increase of DC and AC line voltages. The improvement attained in rectifier AC line voltage in SVC case surpasses that of VDCOL because the SVC is connected at rectifier bus while the VDCOL is installed on current controller at the inverter side. The adopted VDCOL characteristics are illustrated in Fig. (6).
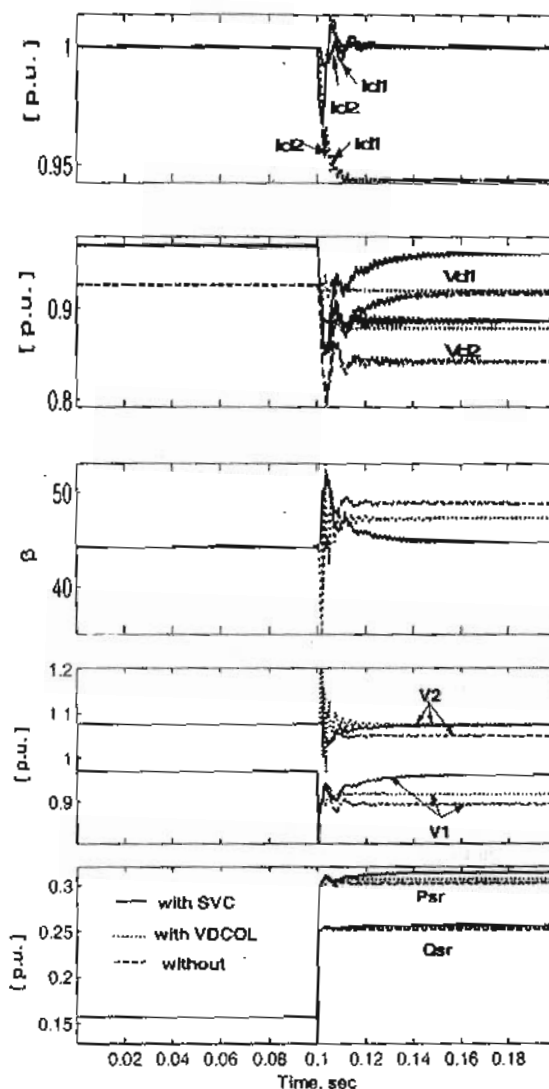

Fig. (5) Transient behavior of AC and DC system parameters with SVC, VDCOL and without any addition in presence of sudden 100% increase of the rectifier's side static load coefficients at 0.1 sec. (SIF at $ESCR_{Rect}$ of 2.9933 on CDA/CC)
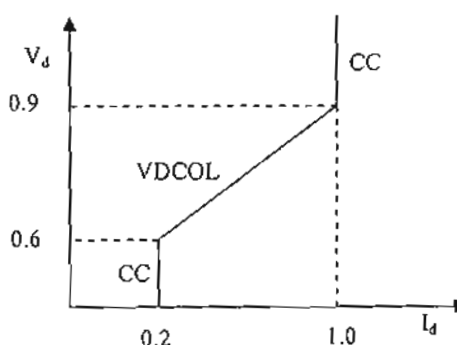

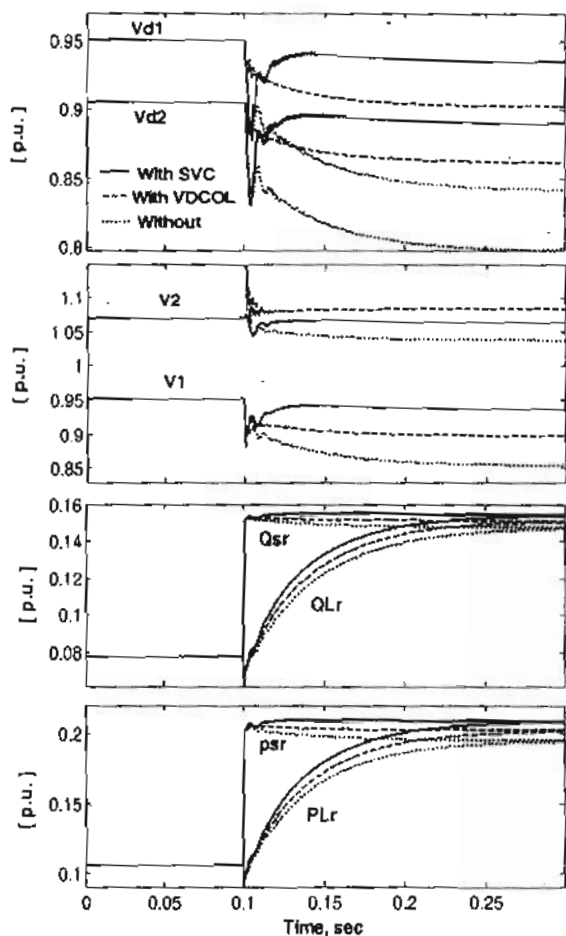Fig. (6) VDCOL control characteristics

Fig. (7) Transient behavior of AC and DC system parameters with SVC, VDCOL and without any addition in presence of sudden 100% increase of the rectifier's side static load coefficients at 0.1 sec., with dynamic loads connected at rectifier bus. (SIF at $ESCR_{Rect}$ of 2.9933 on CDA/CC.)

Fig. (7) illustrates the effect of installing SVC at rectifier AC bus, adding VDCOL and without any addition in the presence of dynamic loads and a sudden increase in static load coefficients. The performance is enhanced due to the action of either of SVC or VDCOL. Nevertheless, the presence of dynamic loads resulted in a degraded performance compared to the case illustrated by Fig. (5).

4.2 Opening AC Line

The AC line connected in parallel in SIFAC configuration has an important effect in system behavior due to the associated active and reactive power transfer between rectifier and inverter. When the parallel AC line is opened, the two AC systems of both rectifier and inverter are separated from each other. Similar phenomenon occurs when the AC line connected between the two inverters of MIF is opened. System power flow equations must be recalculated for the new configuration.
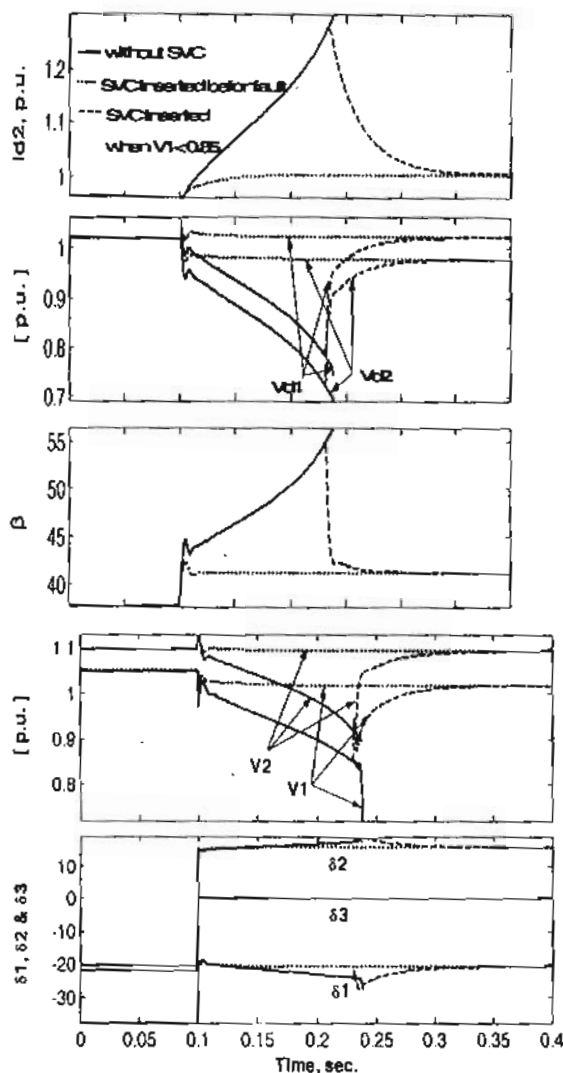

Fig. (8) Transient behavior of AC and DC system parameters with and without SVC due to sudden opening of AC line at t = 0.1 sec in SIFAC (CDA/CP at $ESCR_{Rect}$ 2.1894 and VSF_{Rect} of 0.9583)

Fig. (8) illustrates the effect of opening of the AC line connected in parallel with the DC system with and without correction action. The considered HVDC system adopts CDA/CP control mode at $ESCR_{Rect}$ of 2.1894 and VSF_{Rect} of 0.9583 (weak inverter AC system). The inverter's AC line voltage decreases causing a consequent reduction in DC line voltage. The power controller increases the advance angle (β) to increase the DC line current and maintain the inverter's DC power. When the system is operated without any corrective action, this process is repeated until the system loses its stability. When SVC is already operated at rectifier AC bus, the system returns quickly to steady state after the AC line is opened; due to the reactive power supplied from SVC. While if the SVC was operated after the AC line voltage at rectifier bus becomes lower than 0.85 p.u., the SVC at rectifier AC bus generates reactive power that raises the

AC line voltage and consequently the DC line voltage after about 0.1 sec. The controller then decreases its advance angle to reduce the DC line current maintaining its DC power transfer and preserving system stability.
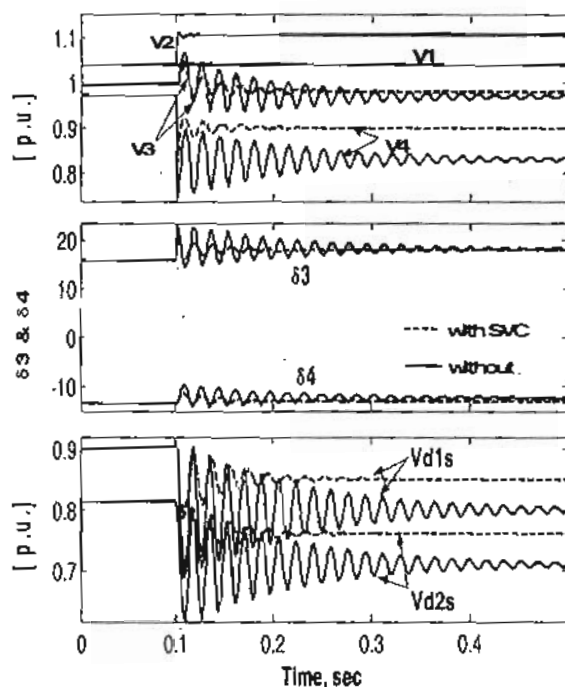

Fig. (9) Transient behavior of AC and DC system parameters due to sudden opening of AC line connecting MIF inverters at 0.1 sec. with and without SVC. (MIF at ESCR$_{Inv}$ of 1.8857, adopting CDA/CC and CC/Cβ for 1st and 2nd DC lines respectively.)

Fig. (9) illustrates the effect of opening the AC line connecting the two inverters in MIF that adopts CDA/CC and CC/Cβ for 1st and 2nd DC lines respectively at ESCR$_{Inv}$ of 1.8857 (weak inverter AC system). Both inverters' AC line voltages decrease causing decreasing of the corresponding DC line voltages. The reduction in line voltage at inverter of second DC line is higher because power transferred through AC is cancelled. Installing an SVC at the inverter of second line improves the AC line voltages and phase angles at both ends of second DC line. No effect appears in AC line voltages and phase angles at both ends of first DC line due to the separation of both AC systems.

4.3 AC Line Voltage Dip

AC line short circuit faults in the neighborhood of the converter bus results in voltage dips. Such reduction in AC line voltage at a converter bus leads to subsequent reduction and increase in DC line's voltage and current respectively, thus degrading system's stability. This condition contradicts that of a DC pole to ground short circuit, where the DC current rises at the rectifier and

decreases at the inverter before the adopted current control mode limits the steady state fault current.

Figs (10) and (11) illustrate the effect of a symmetrical short circuit fault simulated by an AC line voltage dip for SIFAC adopting CDA/CC control mode at both inverter and rectifier sides respectively.
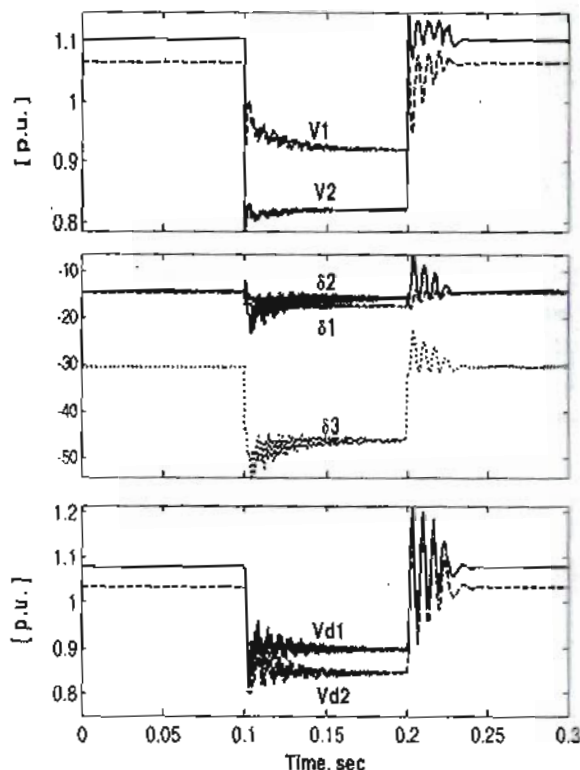

Fig. (10) Transient behaviors of AC and DC system parameters due to 27.27% voltage dip at inverter side (SIFAC on CDA/CC, fault at 0.1 sec, cleared at 0.2 sec)

Fig. (10) illustrates that a reduction in AC line voltage at inverter AC bus is greater than that at rectifier AC bus due to a fault at AC bus near the inverter. The transient responses of AC phase angles and DC line voltages at both rectifier and inverter sides are also illustrated.

Fig. (11) illustrates that the reduction in AC line voltage at AC bus of rectifier is greater than that at the inverter AC bus due to a fault occurring at AC bus near from inverter. It illustrates also the transient responses of AC phase angles and DC line voltages at both rectifier and inverter sides. The effect on phase angle δ_3 is greater than that of δ_1 and δ_2 due to the constant active power transfer from inverter bus to infinite bus in inverter side; which is a constraint of the algebraic equation of active power at infinite bus.
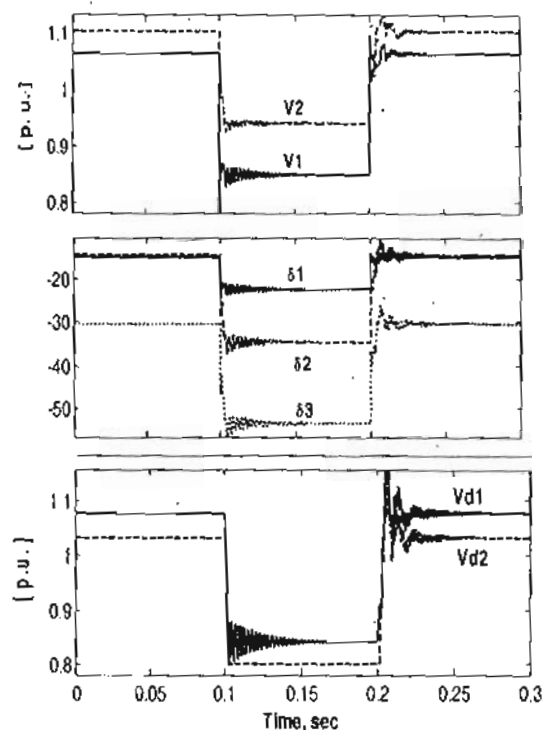
Fig. (11) Transient behaviors of AC and DC system parameters due to 27.27% voltage dip at rectifier side (SIFAC on CDA/CC, fault at 0.1 sec, cleared at 0.2 sec)

5 Conclusions

The HVDC system's behavior when subjected to transient disturbances was modeled and analyzed. Furthermore, based on the presented analysis, the different HVDC system's transient stability enhancement methods and/or corrective control actions are discussed, and their application adequacy and extent are analyzed.

Transient stability of the system is affected by the system's initial operating state, the kind and severity of disturbance, and the response of the HVDC system controls. The transient behavior of HVDC system is improved by injected reactive power at converter bus or by improving HVDC system control characteristics by adopting voltage dependent current order limit effect. The present analysis provides the HVDC system operator with an efficient tool to alleviate overstressing and ensure adequate functionality of the HVDC system.

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LIST OF SYMBOLS

a_{ij}	Converter's transformer tapping ratios; i = "1" for rectifier and "2" for inverter, j = "f" for first line and "s" for second line.
V_{dij},	DC lines voltages at rectifier or inverter.
I_{d1} and I_{d2}	DC line current at rectifier and inverter sides respectively.
$\delta_1, \delta_2,$ δ_3 and δ_4	Line voltage phase angles at rectifier and inverter of first and second DC lines.
α and β	Firing and advance angles of rectifier and inverter sides respectively.
CC,CDA ,Cβ and CP	Constant current, constant rectifier delay angle, constant inverter advance angle, and constant power control respectively.
$ESCR_{Rect}$	Effective short circuit ratio at rectifier
$ESCR_{Inv}$	Effective short circuit ratio at inverter