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MICROPROCESSOR-AIDED ANALOG-TO-DIGITAL CONVERSION

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ABSTRACT:

The use of microprocessors in data conversion is receiving increasing interest. This does not only boost circuits reliability, reduce number of components but it also adds new dimensions in converter design. Software simulation of some complex functions such as successive approximation registers, priority encoders... etc. could be in several cases of advatage.

In this paper two microprocessor-based A/D converter circuits are suggested and tested. With a premitive microcomputer system (University Board TMS 9980) sampling rates of 3257 sample/sec for a 12-bit successive approximation routine and 9416 sample/sec for a 6-bit cyclic-flash structure were obtained. Other measured results are promising and depend mainly on the used comparators. The tested techniques are suitable for a multitude of applications such as computer tomography, digital recording of sound signals ... etc.

INTRODUCTION:

Analog-To-Digital Converters are now used in numeroous applications such as robotics, digital control, computer tomography, telemetry, data storage and/or transmission... etc. Several converter structures are known [1]. Speed, resolution and hardware complexity (cost) are the main parameters of each structure [2] . These parameters are usually contradicting so that a certain structure should be based on which parameter is of interest otherwise a compromise is made.

Thanks the recent develpement in VLSI circuits, several efficient microprocessor chips as well as low-access time high-capacity semiconductor memories are now available at low cost. Therefore simulating as many functions as possible of a certain converter structure via a microcomputer system would result in a respectfull cost and space savings beside providing much more design flexibility.

A 12-bit Successive Approximation A/D Conversion Algorithim

A very suitable A/D conversion technique for microprocessor implementation is the successive approximation technique shown in Fig. 1 . The function of the of the Successive Approximation Register (SAR) is to make a series of gusses for the applied input. For an n-bit resolution n cycles are required before the best

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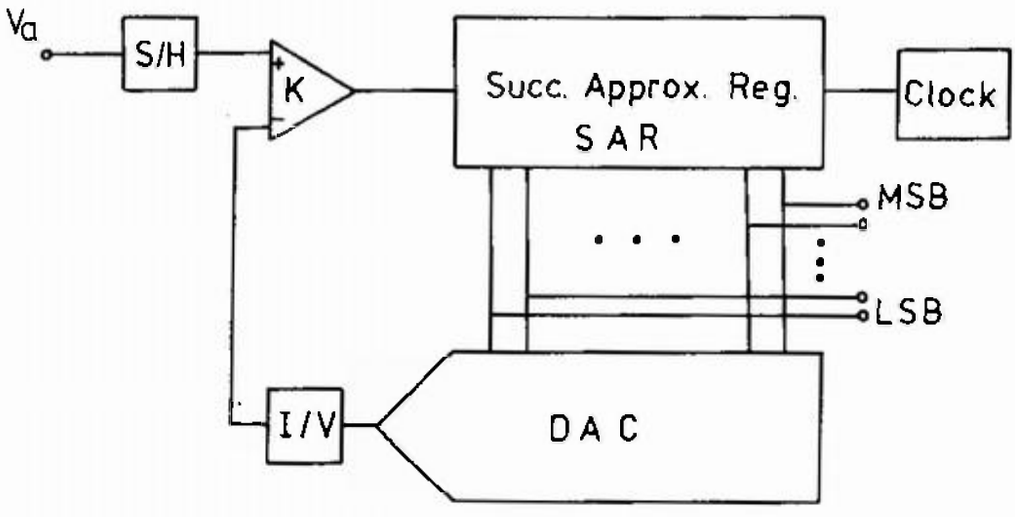

Fig. 1: A Block Diagram of a Successive-Approximation A/D Converter

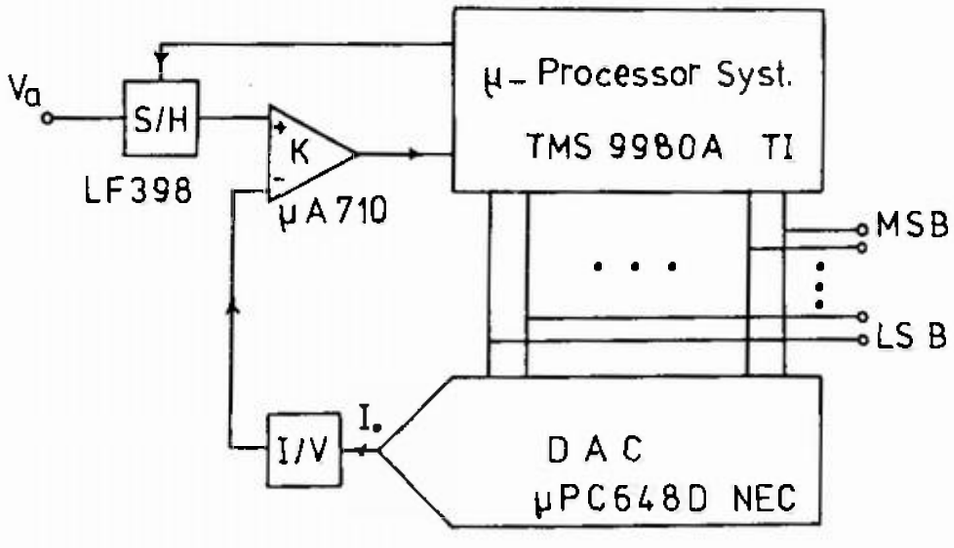

Fig. 2: Microprocessor Implementation of the Succ. Approx. A/D Conversion

estimate is reached. The logic performed by the SAR is to set the i^{th} bit at the start of the i^{th} cycle. This bit together with the bits generated in preceeding cycles are D/A converted and compared with the analog input. Depending on the comparator state, The SAR makes a decision whether to reset such bit, if a change of comparator's state is detected, otherwise it is left high. In a microprocessor-based realization, beside simulating such logic and decision making functions, the highly stable clock source of the system will accordingly replace the timming circuit of a pure hardware realization. The amount of required hardware is thus reduced, as shown in Fig.2, to the comparator, the DAC as well as the processor system (CPU, ROM, RAM, I/O) .

A flow chart of the suggested algorithim for a resolution of 12 bits is given in Fig. 3. The program is written for the TMS 9980 University Board [4] . The procedure starts by resetting all bits and trying to set one bit at a time starting by with the MSB and henthforth untill all bits are exhausted. A block diagram of the system is shown in Fig. 4.

The measured static and dynamic performances of the realised converter are illustrated in table I. The maximum obtainable sampling frequency for a word length of 12 bits was 2.78 kHz. This upper limit is dictated by the machine cycle of the used processor system. However, it represent an improvement compared to other tried algorithims [5]. The measured maximum differential non-linearity, as depicted in Fig. 5, is 0.19 mV which is far below the 1/2 LSB limit. This interesting feature makes such system suitable, for example, for speech encoding applications as in PCM systems.

A 6-bit Multiplexed-Flash A/D Conversion Algorithim

The parallel (Flash) conversion technique provides the highest possible conversion rates [1] yet with the most complex hardware. The required number of comparators, taken as a measure of circuit complexity, for a resolution of n bits is given by

$$N = 2^n - 1$$

Hence, any economical converter structure that is required for high frequency applications should maintain such structure [2,3]. The multiplexed-flash converter structure [3] is a new economical technique that combine the high-speed capabilities of the parallel structure with the hardware simplicity of the cyclic technique. For a word length of n x m bits, a single n-bit flash-type quantizer is used m times in a cyclic manner to provide the output. A block diagram illustrating

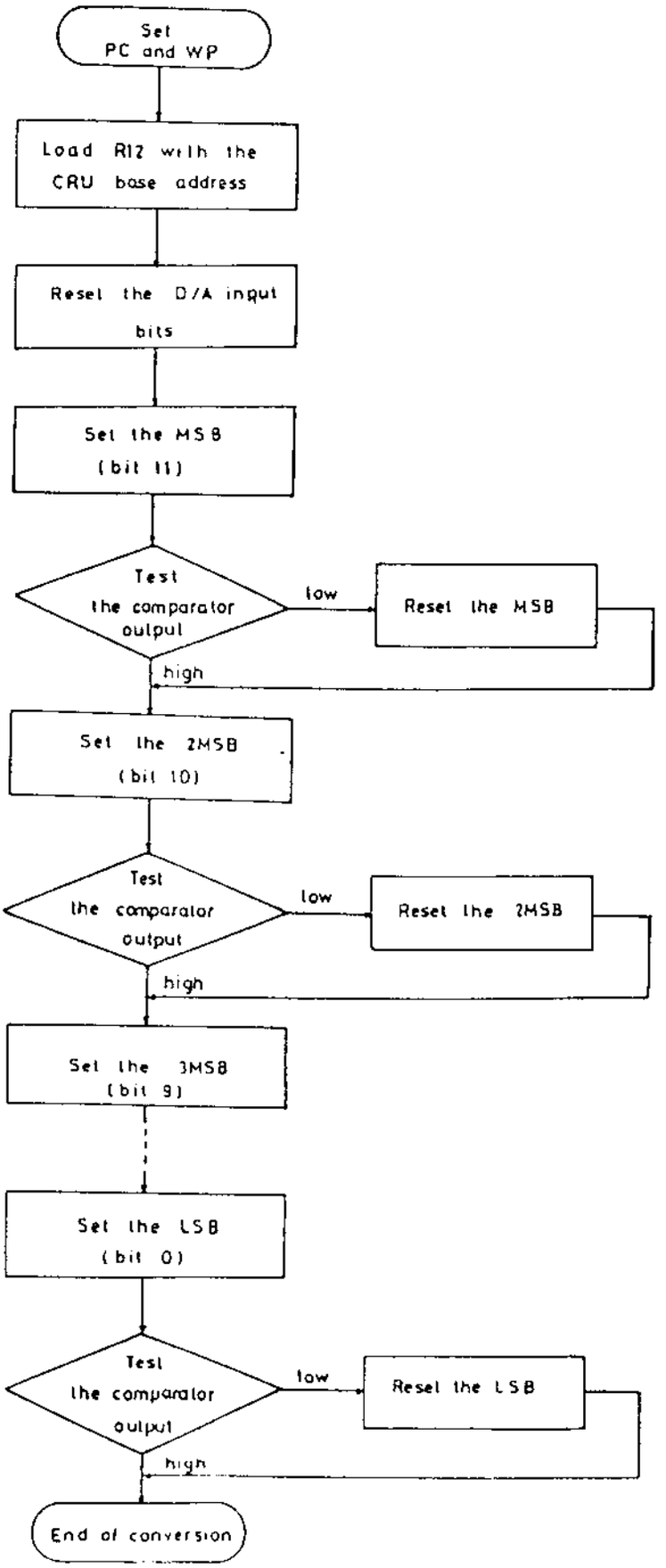

Fig. 3: Flow Chart of the Succ. Approx. Algorithim

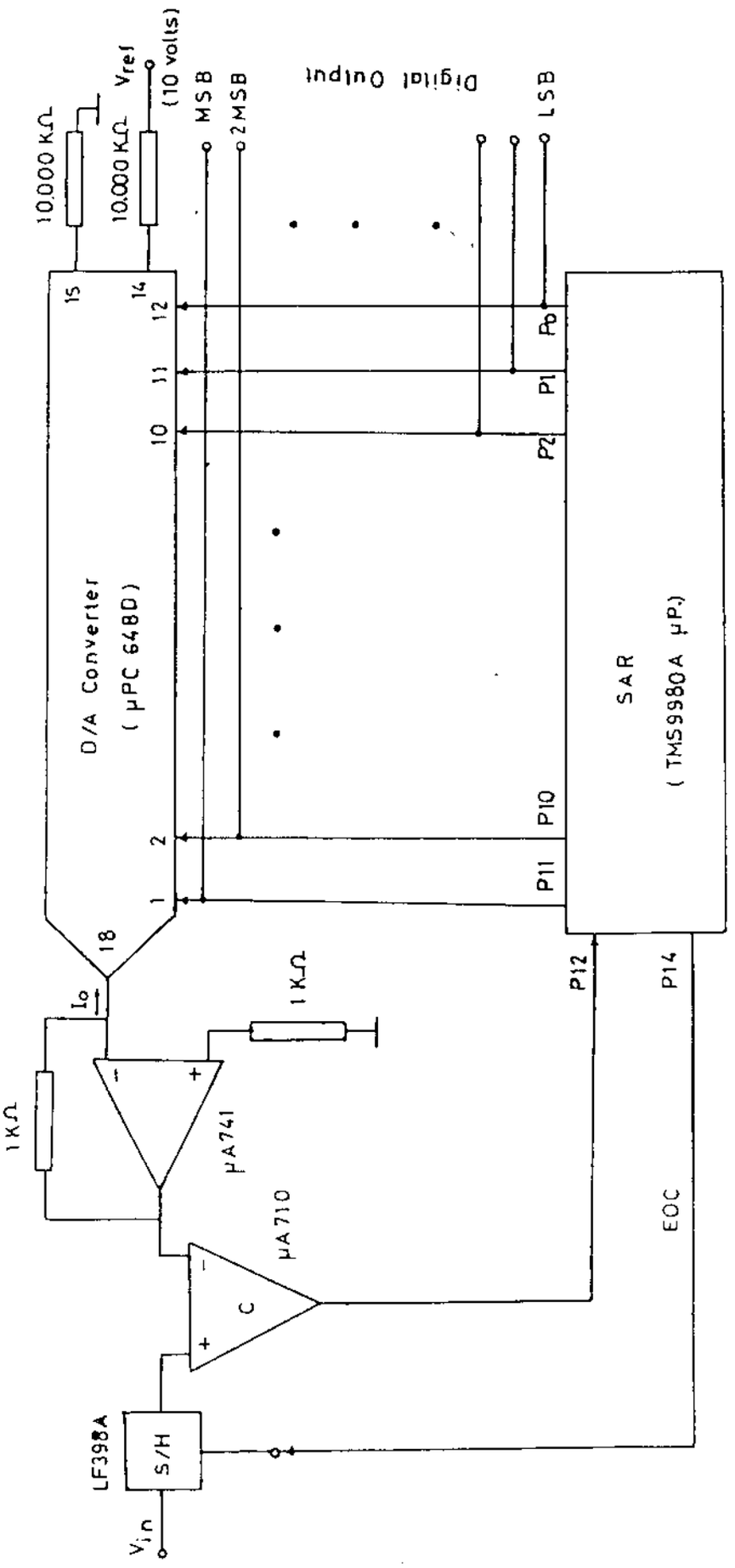

Fig.4 : Block Diagram of a microprocessor realization of a 12-bit Succ. Approx. A/D Converter

Table I : Measured Static and Dynamic Performance
12-Bit Successive Approximation Algorithim

Full-Scale Range	4 V
LSB	0.9766 mV
Full-Scale Error	0.108 mV
Zero-Scale Error	-0.06 mV
Non-Linearity Error(max.)	0.108 mV
Differential non-linearity(max.)	0.19 mV
Conversion Time (12 bits)	307 µSec
Conversion Rate	3257 Conversion/Sec
Apperture Time	26.4 µSec

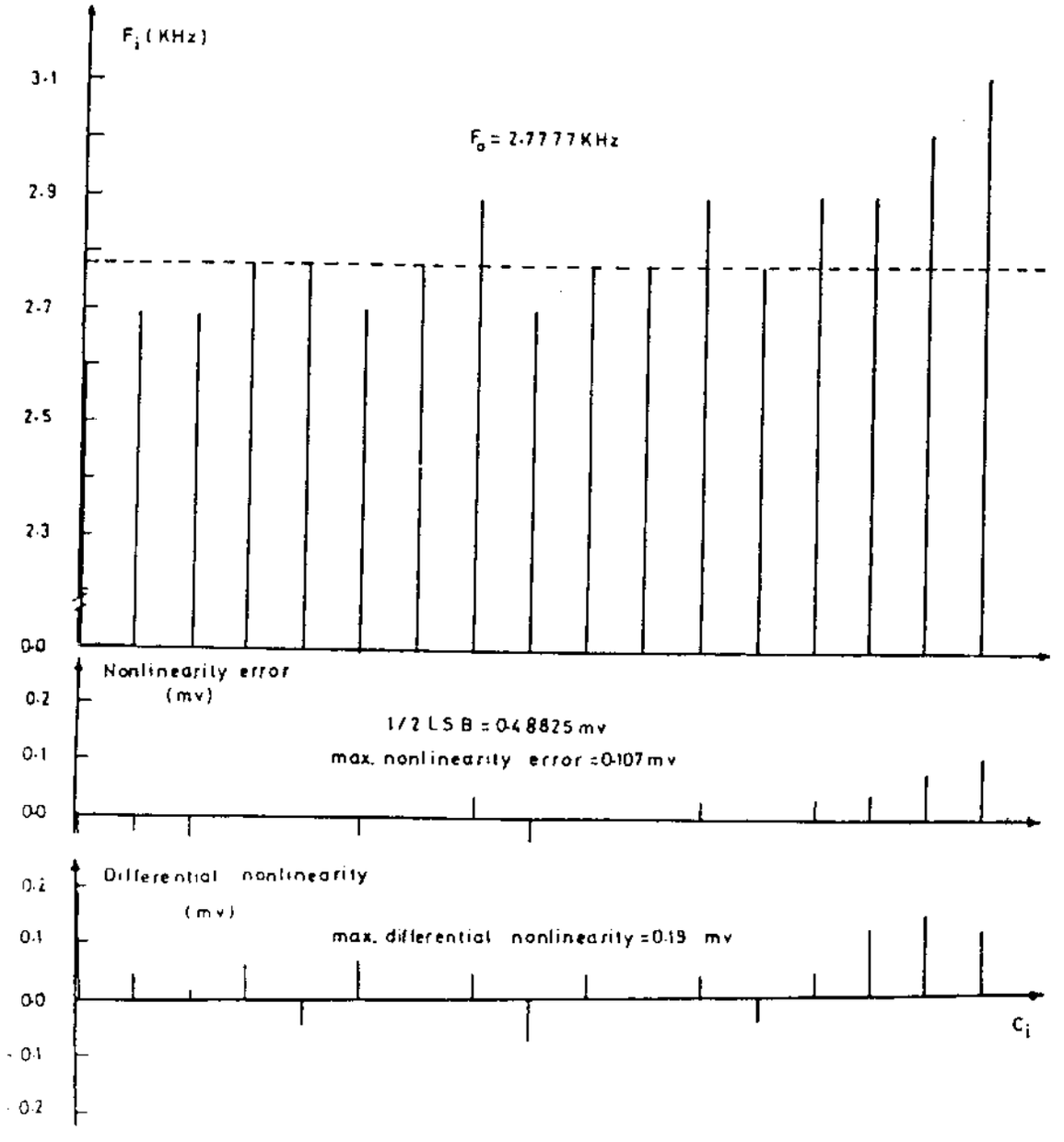

Fig.5 : Measured Differential non-linearity
Succ. Approx. Algorithim

the concept is given in Fig. 6. The bits generated in a preceeding cycle(s) are first D/A converted. The resulting analog output is then subtracted from the applied analog signal to provide an updated input for the next cycles. At the same time an appropriate reference voltage for the quantizer is switched to generate the next n bits and so on. After m cycles the output will be available on a latch. Although the conversion time with this technique, compared to the all parallel solution, is increased m times, a saving in the required number of comparators of :

$$2^{n.m} - 2^{n}$$ is achieved.

Microprocessor implementation of such technique would result in economically feasible realization especially in those cases where high resolution at high speed and/or multi-channel systems are required. In such cases the microprocessor system will provide the complex functions of all the priority encoder, timing,storage, and switching of the proper reference voltages.

Due to the limited I/O ports of the available microprocessor system a resolution of 6 bits eas only possible. A block diagram of the suggested circuit is shown in Fig. 7. The flow chart of the algorithim is given in Fig. 8. Table II summarises the measured static and dynamic chracteristics of the realized converter. It is to be noted here also that the maximum differential non-linearity is well below the 1/2 LSB limit. The maximum possible sampling rate was 9.416 k sample/sec.

CONCLUSION:

Two microprocessor-aided A/D converter designs are suggested and tested. They are much more economical compared to pure parallel realizations especially in multi-channel systems and/or where high resolutions at moderate speeds are required. In such cases the necessary hardware becomes too complex to be economically feasible. The selected resolutions are dictated by the I/O ports of the used microprocessor system. They are used only to demonstrate the effectiveness of teh techniques.

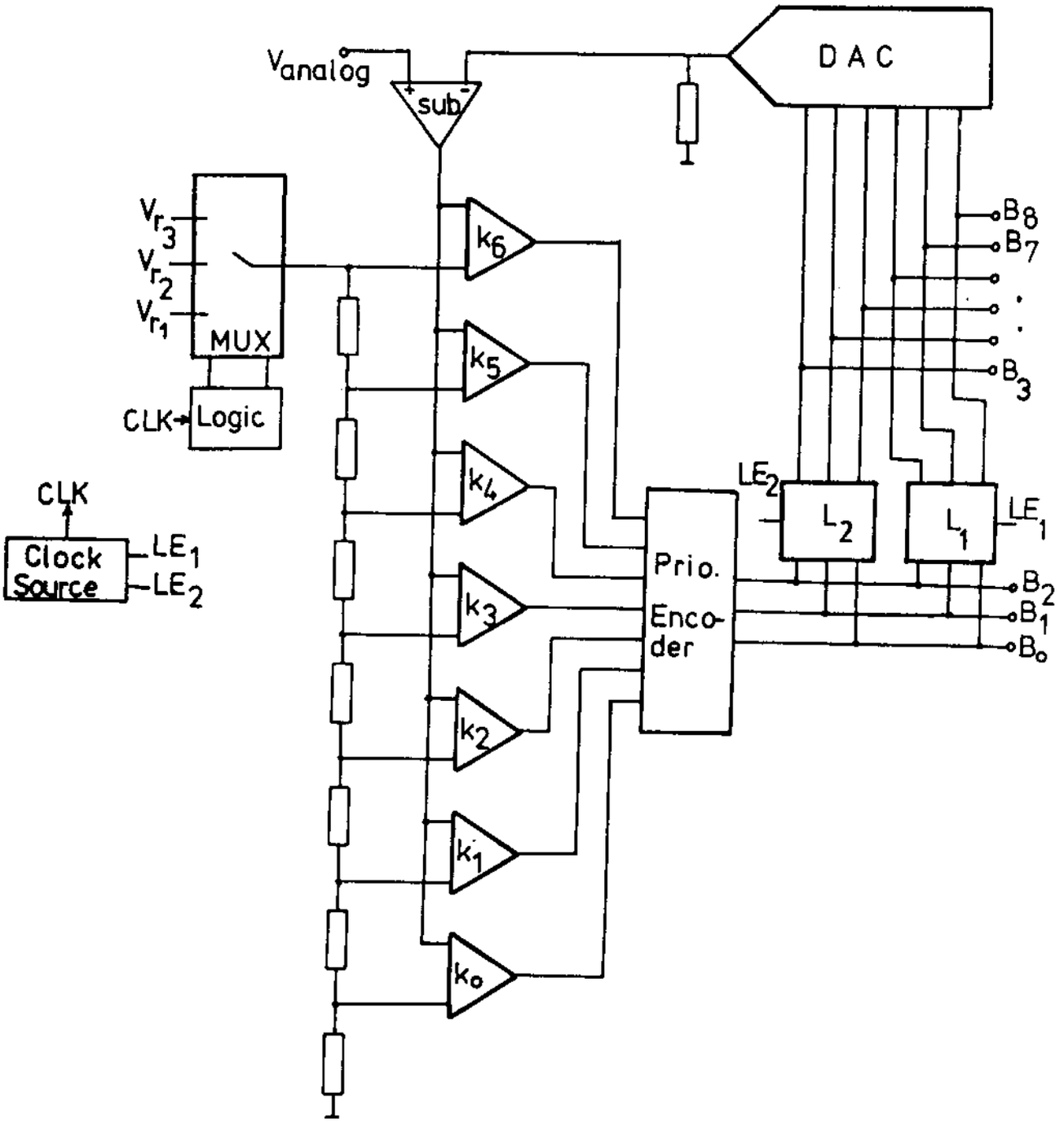

Fig.6 : Block Diagram of the Multiplexed-Flash A/D Converter

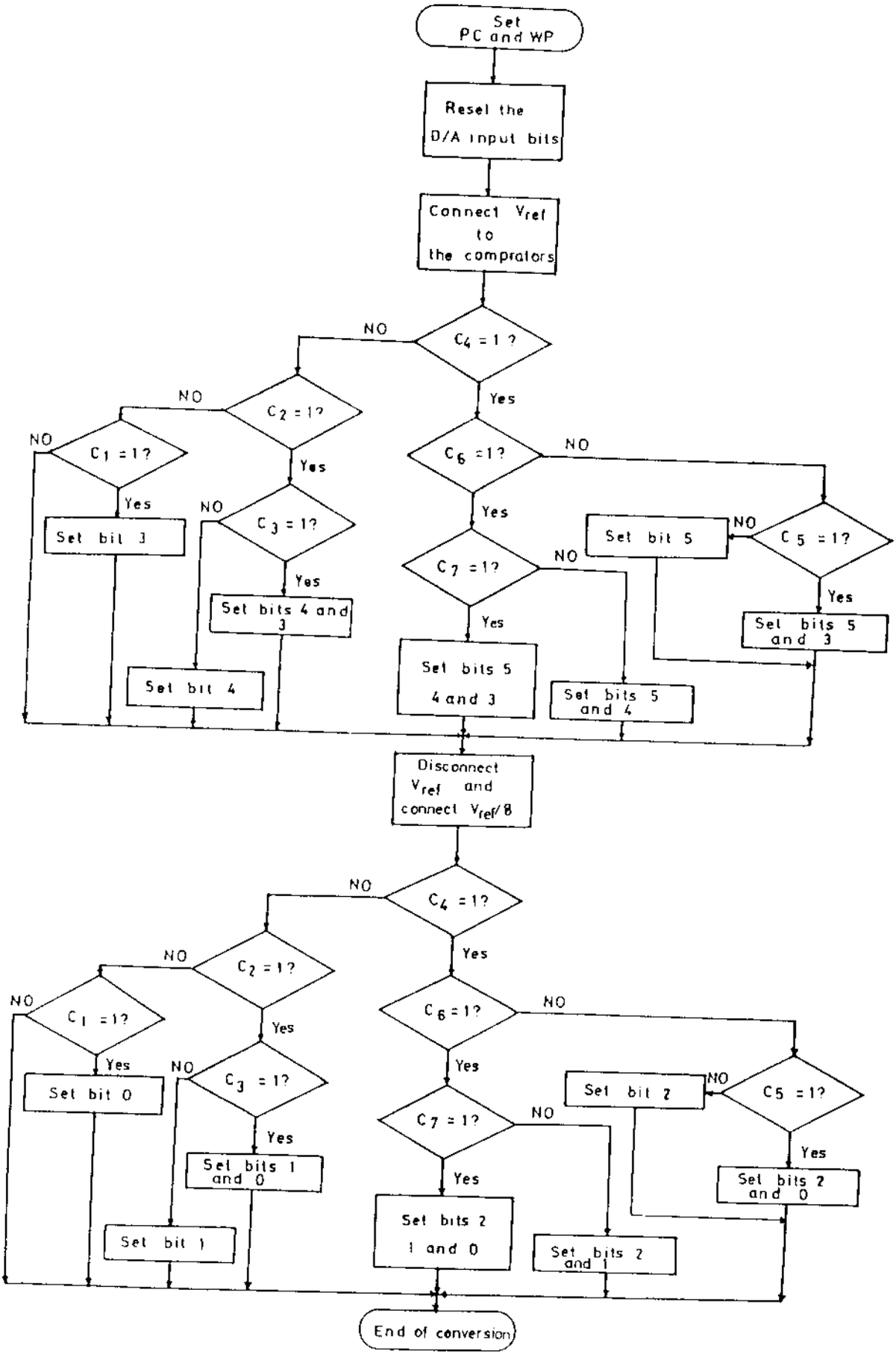

Fig.3 : Flow Chart of the Multiplexed-Flash Algorithim

Table II : Measured Static and Dynamic Performance
6-Bit Multiplex-Flash Algorithim

Full-Scale Range	4 V
LSB	62.5 mV
Full-Scale Error	-10.9 mV
Zero-Scale Error	11.5 mV
Non-Linearity Error (max.)	11.5 mV
Differential non-linearity (max.)	-7.75 mV
Conversion Time	106.2 µSec
Conversion Rate	9416 Conversion/Sec
Apperture Time	20 µSec

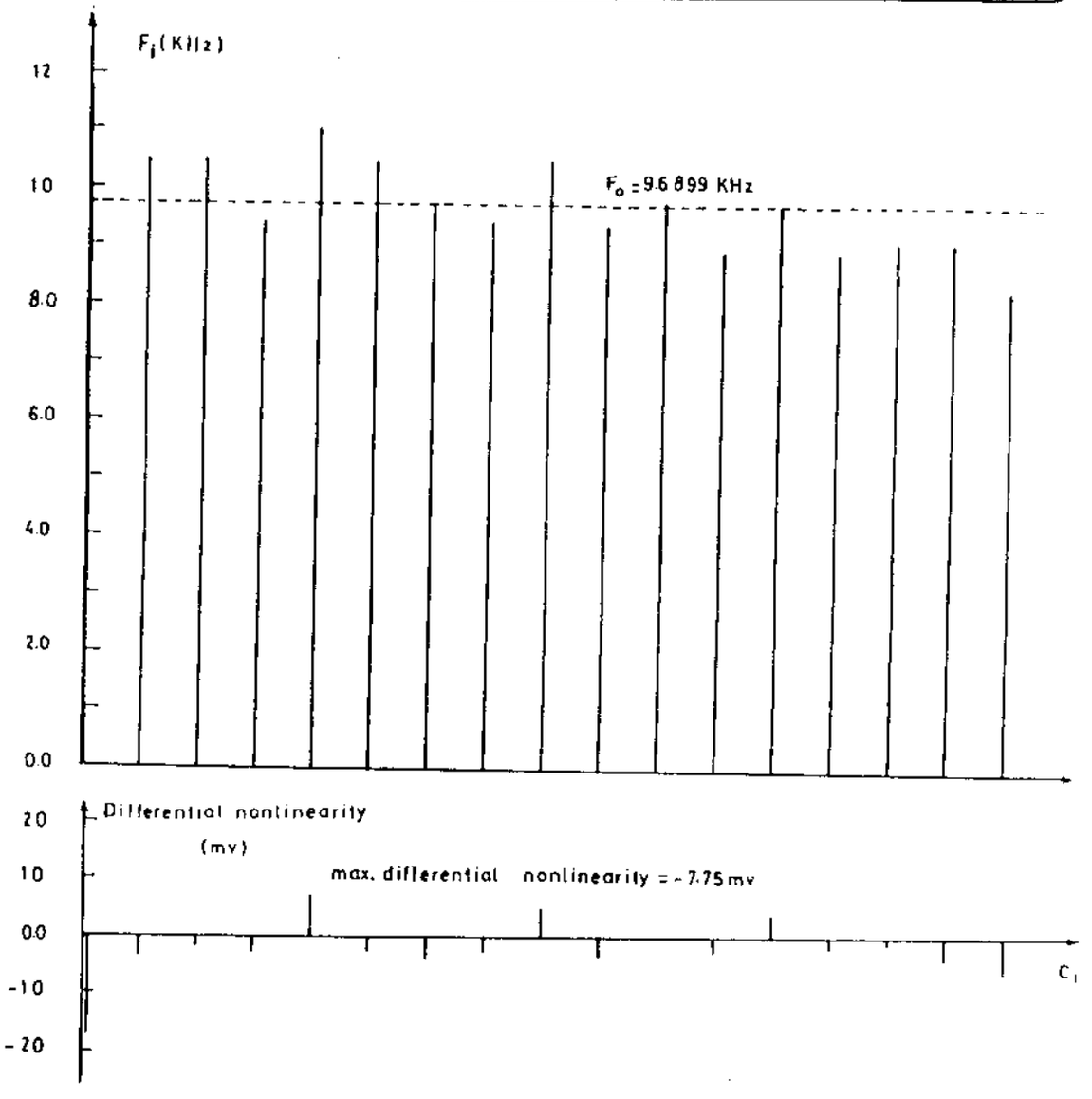

Fig.9 : Measured Differential non-linearity
Multiplexed-Flash Algorithim

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